DISTRIBUTED MICRO INSTRUCTION SET PROCESSOR ARCHITECTURE FOR HIGH-EFFICIENCY SIGNAL PROCESSING

ABSTRACT

A wireless communication system hosts a plurality of processes in accordance with a communication protocol. The system includes application specific instruction set processors (ASISPs) that provided computation support for the process. Each ASISP is capable of executing a subset of the functions of a communication protocol. A scheduler is used to schedule the ASISPs in a time-sliced algorithm so that each ASISP supports several processes. In this architecture, the ASISP actively performs computations for one of the supported processes (active process) at any given time. The state information of each process supported by a particular ASISP is stored in a memory bank that is uniquely associated with the ASISP. When a scheduler instructs an ASISP to change which process is the active process, the state information for the inactivated process is stored in the memory bank and the state information for the newly activated process is retrieved from the memory bank.